6-15-00

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Docket No: NEC DP-624
Date: June 14, 2000

Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor: Sadao Nakayama
For: Semiconductor Storage Device

Enclosed are the following:

[ ] Submission of Incomplete Application
[X] Specification 7 pages; Claims 2 pages; Abstract 1 page
[X] sheet(s) of drawings 2 pages
[X] Declaration and Power of Attorney
[X] Assignment of the invention to NEC Corporation
[ ] Small Entity Statement
[X] A certified copy of Japanese application no. 172387/1999 filed June 18, 1999
[X] Prior Art Statement
[ ] Preliminary Amendment ____ pages

Priority is hereby claimed under 35 USC 119 by way of Japanese patent application Nos. 172387/1999 filed June 18, 1999.

Benefit is hereby claimed under Title 35, United States Code 119(e) of United States provisional application No. _____ filed _____.

The filing fee has been calculated as shown below:

		SMALL ENTITY	LARGE ENTITY
BASIC FEE:		$ 345.00	$ 690.00
TOTAL CLAIMS:	8 - 20 = -0-	x 9 =	x 18 = -0-
INDEPENDENT CLAIMS:	1 - 3 = -0-	x 39 =	x 78 = -0-
MULT. DEPEND. CLAIMS:		+130 =	+ 260 = -0-
TOTAL:		$	$ 690.00

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SEMICONDUCTOR STORAGE DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor storage device. More to particularly, this invention relates to wiring structure of the semiconductor storage device according to stack type MCP (Multi Chip Package) of superimposing a plurality of chips.

Description of the Prior Art

Formerly, the stack MCP to be package is formed in such a way that a plurality of chips are superimposed. Namely, the stack MCP consists of the package of causing a plurality of chips to be superimposed. In the stack MCP, generally, a bonding pad of respective chips is arranged in a place near by, with the same arrangement. Further, it is necessary that respective chip sizes are the optimum size. In recent years, it is required combination of memory with various capacities.

In order to reply this requirement, for instance, the Japanese Patent Application Laid-Open No. HEI 5-121643 discloses bonding method. Such the bonding method is that bonding is performed at the position where bonding pad position of the chip side is shifted largely.

Fig. 1 is a view showing a conventional stack MCP.

In Fig. 1, a package substrate 1, a lower chip 2, and an upper chip 3 are placed one upon another while being shifted from the lowest layer. A bonding pad 4 of the upper chip 3 is connected to a bonding pad 5 of the package substrate 1 by a bonding wire 6. A bonding pad 7 of the lower chip 2 is connected to a bonding pad 5 of the package substrate 3 by a bonding wire 8.

As described above, in the conventional stack MCP, the bonding wire 6 from the upper chip 3 is connected directly to the package substrate 1 exceeding the lower chip 2, therefore, extremely long bonding wire 3 is necessary. For that reason, the bonding wire 3 deviates from

prescribed position on the occasion of confining to be enclosed the bonding wire according to the resin, thus there is the problem of existing danger of the breaking down of a wire or contact of another wire therebetween.

Further, there is the problem that thickness of the package is forced to be increased because the bonding wire increases in the height direction for the sake of wire bonding of long distance.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention, in order to overcome the above-mentioned problem to provide a semiconductor storage device which enables various plural memories to be mounted on the same package, further in the case where even though scale of respective chips and / or position of the bonding pad are different, it is capable of providing the stack MCP in which the chips are superimposed.

According to a first aspect of the present invention, in order to achieve the above-mentioned object, there is provided a semiconductor storage device constituted in such a way that it causes a lower chip and an upper chip are superimposed on a substrate, which comprises a wiring substrate for relaying electric connection between the upper chip and the substrate which wiring substrate is provided between the lower chip and the upper chip.

According to a second aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein there are provided a first terminal connected to a terminal on a surface of the upper chip, a second terminal connected to a terminal on a surface of the substrate, and a wiring pattern for connecting the first and the second terminals on the surface of the wiring substrate.

According to a third aspect of the present invention, in the second aspect, there is provided a semiconductor storage device, which further

comprises a first bonding wire for connecting the terminal of the surface of the upper chip with the first terminal, and a second bonding wire for connecting the terminal of the surface of the substrate with the second terminal.

According to a fourth aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein there is provided a wiring pattern whose one end is connected to a terminal on a rear surface of the upper chip, and whose other terminal is connected to a terminal on a surface of the lower chip.

According to a fifth aspect of the present invention, in the second or the fourth aspect, there is provided a semiconductor storage device, wherein the terminal of the surface of the lower chip is connected to the terminal of the surface of the substrate by a third bonding wire.

According to a sixth aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein the wiring substrate is sheet shape wiring substrate.

According to a seventh aspect of the present invention, in the first aspect, there is provided a semiconductor storage device, wherein the wiring substrate is board shape wiring substrate.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with accompanying drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limit of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a constitution view showing conventional stack MCP;

Fig. 2 is a constitution view showing a first embodiment of the present invention;

Fig. 3 is a constitution view showing a second embodiment of the present invention; and

Fig. 4 is an enlarged fragmentary view of Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described in detail in accordance with the accompanying drawings.

Fig. 2 shows constitution of the stack MCP (Multi Chip Package) according to the first embodiment of the present invention. The present embodiment, as illustrated, characterized in that, in the stack type MCP, a wiring sheet 9 intervenes between an upper chip 3 and lower chip 2, thus the bonding wires 10, 11 are connected from the upper chip 3 to the package substrate 1 while relaying this wiring sheet 9.

Namely, in Fig. 2, there is provided the wiring sheet 9 between the upper chip 3 and the lower chip 2. There are provided a first bonding pad 12 and a second bonding pad 13 at the wiring sheet 9. Further, there is provided a wiring pattern 14 for connecting these bonding pads 12, 13. Furthermore, the bonding pad 4 of the upper chip 3 is connected to the above-described bonding pad 12 by the first bonding wire 10. Moreover, the second bonding pad thirteen is connected to the bonding pad 5 of the package substrate 1 by the bonding wire 11.

According to the above constitution, the signal from the upper chip 3 is transmitted to the package substrate 1 while relaying the wiring sheet 9. Namely, the signal from the upper chip 3 is transmitted to the bonding pad 4, the bonding wire 10, the bonding pad 12, the wiring pattern 14, the bonding pad 13, the bonding wire 11, and the bonding pad 5. Oppositely, transmission of the signal from the package substrate 1 to the upper chip is implemented in the opposite order to the order described above.

Consequently, according to the present embodiment, in the case

where a differential of chip size is large between the upper chip 3 and the lower chip 2, wire length does not become long, thus it is capable of avoiding the problem concerning the package combination such as wire deviation and so forth described above. Further, in large number of cases, the stack MCP shares the signal both of the upper chip 3 and the lower chip 2, combination between chips whose arrangement of the bonding pads becomes easy by employing the wiring substrate 9. Namely, due to the wiring pattern 14 on the wiring sheet 9, it is capable of putting the wire of the upper chip 3 to periphery of the bonding pad 7 of the lower chip 2 through which the common signal flows.

Next, there will be described the second embodiment of the present invention. In the above-described the first embodiment, the constitution is that it causes rear surface of the upper chip 3 to be placed on the surface of the wiring sheet 9. However, in the present embodiment, the upper chip 3 is placed on the wiring sheet 9 in such a way that chip surface is directed to the lower direction while causing inside and outside to be reversed before placing on the wiring sheet 9. Further, one end of the wiring pattern 14 of the wiring sheet 9 is connected directly to the bonding pad 4 of the upper chip 3, while the other end of the wiring pattern 14 is connected to the bonding pad 7 of the lower chip 2.

According to the above-described constitution, the bonding pad 4 is connected directly to the wiring pattern 14 on the wiring sheet 9. Consequently, the bonding falls into disuse with respect to the wiring sheet 9 from the upper chip 3.

Further, it causes the wiring pattern on the wiring sheet 9 to be lengthened to the upper part of the bonding pad 7 of the lower chip 2, thus forming the pad such that the bonding pad 7 of the lower chip 2 exposes. Thereby, as shown in Fig. 4, it becomes possible to perform bonding both of the bonding pad 7 of the lower chip 2 and the wiring pattern 14 on the wiring sheet 9 to the bonding pad 5 of the package substrate 3 with one

time of wire bonding.

As described above, according to the present embodiment, it becomes to remove the wire bonding with respect to the wiring sheet 9 from the upper chip 3, it is capable of getting thin the package further. As shown in Fig. 3, when the arrangement of the bonding pad 4 of the upper chip 3 is perpendicular to the arrangement of the wiring sheet 9, the lower chip 2, and respective bonding pad of the package substrate 1 in the horizontal direction, since it becomes to remove the wiring bonding to the horizontal direction, there is obtained the effect of causing size of the horizontal direction of the package to be reduced.

Further, in the above described the first and the second embodiments, description is implemented with respect to wiring sheet as the wiring substrate, however, it is also suitable that the wiring substrate is board type one.

As described above, according to the present invention, there is provided the wiring substrate such as the wiring sheet and so forth between the upper chip and the lower chip, thus causing electric connection to the package substrate from the upper chip to be implemented through the above described wiring substrate, therefore, even though the differential of the chip size between the upper chip and the lower chip is large, it becomes possible to move the bonding pad to the ideal bonding position.

For that reason, it is capable of developing easily the stack MCP of chips of combination which it is impossible to assemble until now because the differential of the chip size is large.

Consequently, it is capable of mounting various plural memories on the same package, thus even though when scale of respective chips and / the position of the bonding pad are different, it is capable of providing the stack MCP in which the chips are superimposed.

Further, in the cases where the upper chip and the lower chip are

performed bonding to the same bonding pad on the package substrate, even though respective chip layouts are different and the bonding pads on the chip exist in the positions with long distance, it is capable of arranging the bonding pad by changing wiring on the wiring sheet to the ideal bonding position.

While preferred embodiments of the invention have been described using specific terms, the description has been for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor storage device constituted in such a way that it causes a lower chip and an upper chip are superimposed on a substrate comprising:

a wiring substrate for relaying electric connection between said upper chip and said substrate which wiring substrate is provided between said lower chip and said upper chip.

2. A semiconductor storage device as claimed in claim 1, wherein there are provided a first terminal connected to a terminal on a surface of said upper chip, a second terminal connected to a terminal on a surface of said substrate, and a wiring pattern for connecting said first and said second terminals on the surface of said wiring substrate.

3. A semiconductor storage device as claimed in claim 2, further comprising:

a first bonding wire for connecting said terminal of the surface of said upper chip with said first terminal; and

a second bonding wire for connecting said terminal of the surface of said substrate with said second terminal.

4. A semiconductor storage device as claimed in claim 1, wherein there is provided a wiring pattern whose one end is connected to a terminal on a rear surface of said upper chip, and whose other terminal is connected to a terminal on a surface of said lower chip.

5. A semiconductor storage device as claimed in claim 2, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

6. A semiconductor storage device as claimed in claim 4, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

7. A semiconductor storage device as claimed in claim 1, wherein said wiring substrate is sheet shape wiring substrate.

8. A semiconductor storage device as claimed in claim 1, wherein said wiring substrate is board shape wiring substrate.

ABSTRACT OF THE DISCLOSURE

A semiconductor storage device enables various plural memories to be mounted on the same package, and even though size of respective chips and / or position of bonding pad are different, it is capable of providing a stack MCP in which the chips are superimposed. It causes wiring sheet to intervene between an upper chip and a lower chip. There are provided a bonding pad 12, a bonding pad 13, and a wiring pattern for connecting these bonding pads in the wiring sheet. A bonding pad 4 of the upper chip is connected to the bonding pad 12 by a first bonding wire, while the bonding pad 13 is connected to a bonding pad 5 of the package substrate by a second bonding wire. According to this constitution, the signal from the upper chip is transmitted to the package substrate while relaying by the wiring sheet.

FIG. 1 PRIOR ART

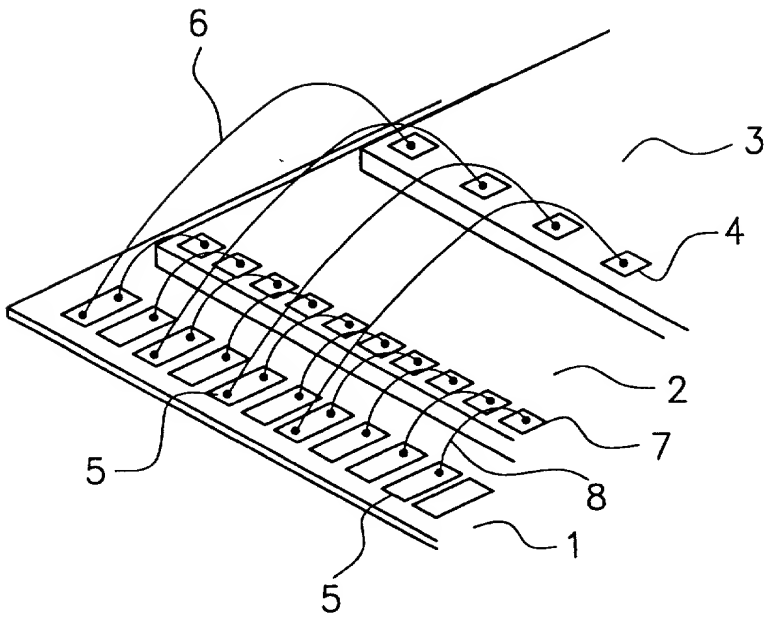


FIG. 2

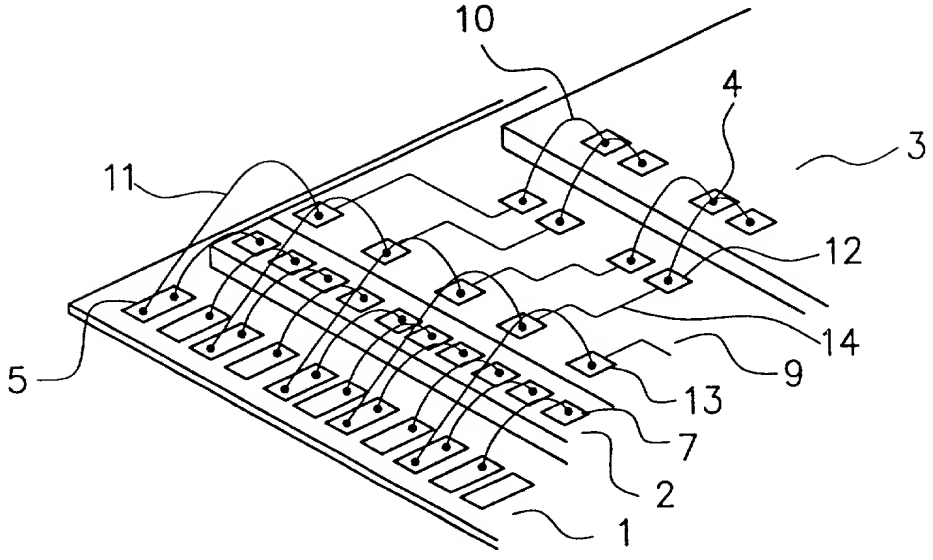


FIG. 3

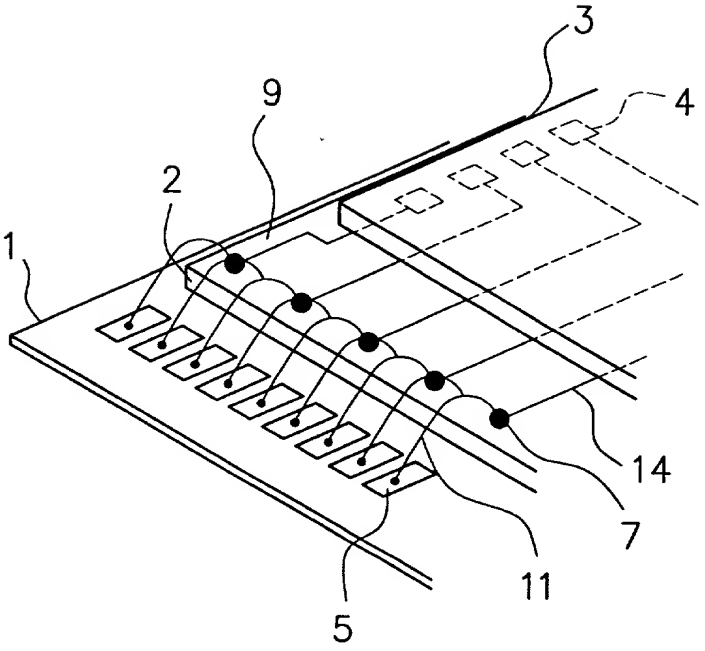
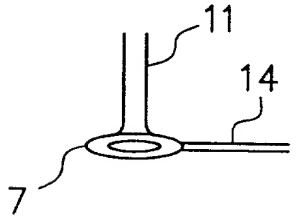


FIG. 4



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SEMICONDUCTOR STORAGE DEVICE

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, S. 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, S.119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
172387/1999 (number)	Japan (country)	18/6/1999 Day/Mo/Yr filed	[X] Yes [ ] No
(number)	(country)	Day/Mo/Yr filed	[ ] Yes [ ] No
(number)	(country)	Day/Mo/Yr filed	[ ] Yes [ ] No

And I hereby appoint HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., a firm composed of Oliver W. Hayes, Reg. No. 15,867; Norman P. Soloway, Reg. No. 24,315; William O. Hennessey, Reg. No. 32,032; Susan H. Hage, Reg. No. 29,646; Steven J. Grossman, Reg. No. 35,001; and ~~Christopher K. Gagne, Reg. No. 36,142~~, or any of them, of 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith.

Please direct all future correspondence in connection with this application to the attention of Norman P. Soloway, Esq., HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Second Inventor's signature _____ Date _____
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Post Office Address _____

Full name of third joint inventor, if any _____
Third Inventor's signature _____ Date _____
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Citizenship _____
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Fourth Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____

Full name of fifth joint inventor, if any _____
Fifth Inventor's signature _____ Date _____
Residence _____
Citizenship _____
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